UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,836	03/30/2004	Kodalapura Nagabhushana Rao Nagaraju	884.B46US1	3122

21186 7590 04/17/2007

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
KENDALL, CHUCK O	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,836	RAO NAGARAJU ET AL.	
	Examiner	Art Unit	
	Chuck O. Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This action is in response to the application filed 03/30/04.

2. Claims 1 – 28 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1 – 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Bogle et al. US 6,353,923 B1.

Regarding claims 1 and 20, Bogle anticipates a method, comprising:

dynamically establishing a first debugging session with a first processing core of a processor (FIG. 4, 422);

dynamically establishing a second debugging session with a second processing core of the same processor (FIG, 4, 423); and

concurrently managing the first and second debugging sessions independently from one another on the same processor (FIG.4, 411).

Regarding claims 2 and 22, the method of claim 1, further comprising:

initiating a first instance of a debugger on the first processing core of the processor for interactions occurring during the first debugging session (FIG.6, 612); and

initiating a second instance of the debugger on the second processing core of the processor for interactions occurring during the second debugging session (FIG.6, 612).

Regarding claims 3,18 and 23, the method of claim 1, wherein dynamically establishing the first and second debugging sessions further comprises dynamically establishing the sessions by connecting the first and second processing cores of the processor to separate instances of a debugger via a Peripheral Component Interconnect (PCI) interface (5: 40 – 55).

Regarding claims 4 and 24, the method of claim 1, further comprising:

debugging a first application within the first debugging session on the first accessing core of the processor (FIG. 411); and

simultaneously debugging a second application within the second debugging session on the second processing core of the processor (FIG. 4, 220 and 230).

Regarding claim 5, the method of claim 1, further comprising:

identifying within a first configuration file of a first debugger the first processing core associated with the first debugging session (FIG. 4, see Host process a); and

identifying within a second configuration file of a second debugger the second processing core associated with the second debugging session (FIG. 2, see Host Process c).

Regarding claim 6, the method of claim 5, further comprising:

routing, by the processor, the first debugger to the first processing core for establishing the first debugging session based on the first configuration file (FIG. 2, see process a, b and c and see control flow which goes in both directions and all associated text); and

routing, by the processor, the second debugger to the second processing core for establishing the second debugging session based on the second configuration (FIG. 2, see process a, b and c and see control flow which goes in both directions and all associated text).

Regarding claim 7, the method of claim 1, further comprising maintaining, by the processor, processor states while dynamically establishing the first and second debugging session (14:5 – 10).

Regarding claims 8, 15 and 25 Bogle anticipates a method/system, comprising:

receiving, by a processor, a first debugging session request (FIG. 4, 422);

receiving, by the processor, a second debugging session request (FIG. 4, 423);

dynamically attaching a first debugger to a first processing core for servicing the first debugging session request (FIG.6, 612 and all associated text); and

dynamically attaching a second debugger to a second processing core for servicing the second debugging request (FIG.6, 612 and all associated text).

Regarding claims 9 and 26, the method of claim 8, wherein dynamically attaching the first and second debuggers further includes identifying the first and second debuggers as a same debugger being initiated as independent and duplicative instances on different processing cores (FIG.6, 612, see all associated text).

Regarding claims 10 and 27, the method of claim 8, further comprising identifying within the first and the second debugging session requests configuration information which identifies the first and second processing cores (FIG. 4, 220 and 230).

Regarding claims 11, 19, the method of claim 8, wherein dynamically attaching the first and second debuggers further includes maintaining a previous state associated with the processor of the first and second processing cores before and after attaching the first and second debuggers to their respective processing cores (FIG. 2, see process a, b and c and see control flow which goes in both directions and all associated text).

Regarding claim 12, the method of claim 8, wherein receiving the first and second debugging session requests further includes remotely initiating the requests from the processor that has the first and second processing cores (FIG.4, see host process b and all associated text).

Regarding claim 13, the method of claim 8, further comprising maintaining existing states associated with existing applications, the existing applications processing on the first and second processing cores before and after dynamically attaching the first and second debuggers to the first and second processing cores, respectively (FIG. 4, 220 and 203).

Regarding claim 14, the method of claim 8, wherein dynamically attaching the first and second debuggers further includes attaching the first and second debuggers to their respective processing cores as their respective processing cores are processing a Number of other applications (FIG. 4, 220 and 203 and all associated text).

Regarding claim 16, the system of claim 15, further comprising a Peripheral Component Interconnect (PCI) interfaced to the processor for receiving requests to dynamically attach the first and second debugger instances to their respective processing cores (5: 40 – 55).

Regarding claim 17 and 28, the system of claim 15, further comprising a first configuration file associated with the first debugging instance and a second configuration file associated with the second debugging instance, wherein each configuration file identifies its respective processing core, and wherein the processor in

response to the configuration files dynamically attaches the debugger instances to their respective processing cores (FIG. 4, 220, 230).

Regarding claim 21, the medium of claim 20, further including instructions for concurrently managing the first and second debugging sessions independent from one another on a processor having the first and second processing cores (FIG. 4, 220 and 230).

Correspondence information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-2723698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-2723695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/18/07